ENGLISH

Synchronisation with DI

Clock can be synchronized by reading minute pulses from digital inputs, virtual inputs or virtual outputs. Sync source is selected with **SyncDI** setting.

When rising edge is detected from the selected input, system clock is adjusted to the nearest minute. Length of digital input pulse should be at least 50 ms. Delay of the selected digital input should be set to zero.

Synchronisation correction

If the sync source has a known offset delay, it can be compensated with **SyOS** setting. This is useful for compensating hardware delays or transfer delays of communication protocols. A positive value will compensate a lagging external sync and communication delays. A negative value will compensate any leading offset of the external synch source.

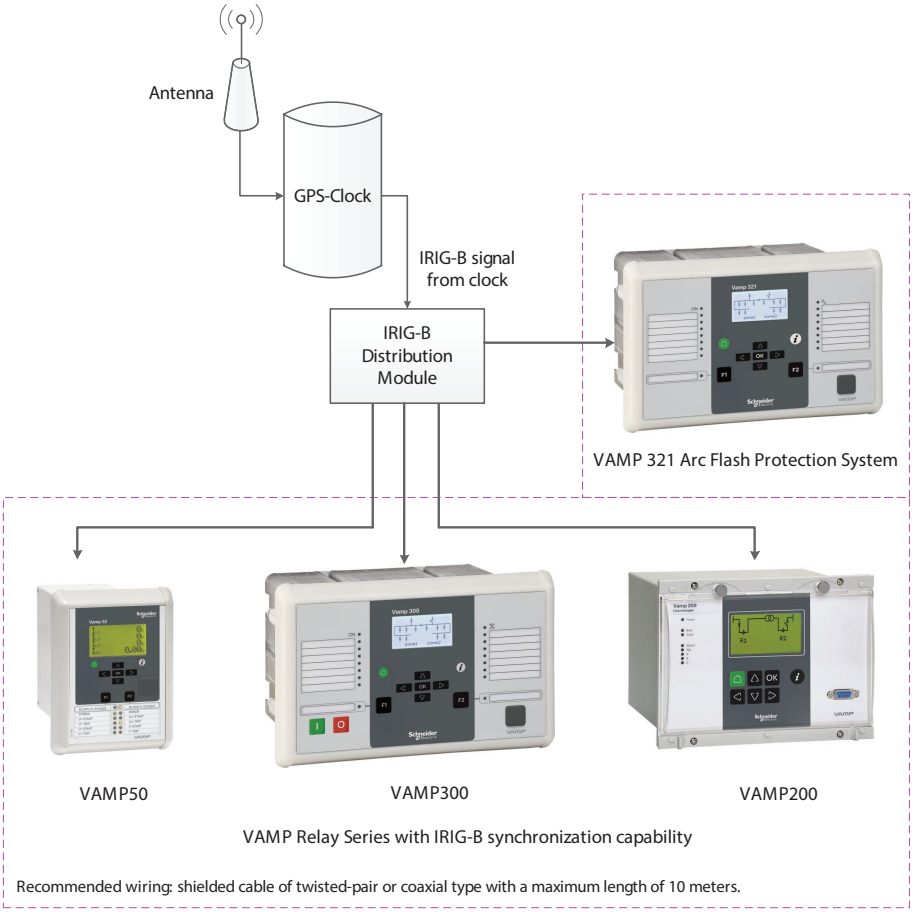
Sync source

When the device receives new sync message, the sync source display is updated. If no new sync messages are received within next 1.5 minutes, the device will change to internal sync mode.

Sync source: IRIG-B003

IRIG-B003 synchronization is supported with a dedicated communication option with either a two-pole or two pins in a D9 rear connector (See Order information on page 179).

IRIG-B003 input clock signal voltage level is TLL. The input clock signal originated in the GPS receiver must be taken to multiple relays trough an IRIG-B distribution module. This module acts as a centralized unit for a point-to-multiple point connection. Note: Daysi chain connection of IRIG-B signal inputs in multiple relays must be avoided.



The recommended cable must be shielded and either of coaxial or twisted pair type. Its length should not exceed a maximum of 10 meters.

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